AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A port independent data transaction interface for multi-port devices, comprising:

a command channel that receives command data and a source id, the source id indicating a source device that transmitted the command data;

a data-in channel having a data-in transfer storage that receives write data and a write source id, the write source id indicating a source device that transmitted the write data, the data-in channel having a data path that circumvents the data-in transfer storage; and

a data-out channel that provides read data and a read id, the read id indicating a source device that transmitted a read command corresponding to the read data.

2. (original) A port independent data transaction interface as recited in claim 1, wherein the source id is utilized to associate command data with corresponding write data.

3. (currently amended) A port independent data transaction interface as recited in claim 2, wherein the write data transmitted to the data-in channel and corresponding command data transmitted to the ~~he~~ command channel are processed when transmitted during different clock signals.

4. (original) A port independent data transaction interface as recited in claim 1, wherein the command channel further receives length data indicating a size of data corresponding to the command data, wherein the length data can indicate an arbitrary data size.

5. (original) A port independent data transaction interface as recited in claim 4, wherein the command channel further receives address data indicating an address associated with data corresponding to the command data, wherein the address data can indicate an arbitrary starting location.

6. (original) A port independent data transaction interface as recited in claim 1, wherein the command channel further receives a priority value indicating a priority level of the command data.

7. (original) A port independent data transaction interface as recited in claim 6, wherein command data is processed based on an associated priority value.

8. (currently amended) A multi-port memory controller having port independent data transaction interface, comprising:

a command transfer storage that receives command data and a source id, the source id indicating a source device that transmitted the command data;

a data-in transfer storage that receives write data and a write source id, the write source id indicating a source device that transmitted the write data, the data-in transfer storage being in communication with a separate data-in signal for each source device coupled to the multi-port memory controller, each data-in signal being further coupled to a data path that circumvents the data-in transfer storage; and

a data-out transfer storage that provides read data and a read id, the read id indicating a source device that transmitted a read command corresponding to the read data.

9. (original) A multi-port memory controller as recited in claim 8, wherein the source id is utilized to associate command data with corresponding write data.

10. (original) A multi-port memory controller as recited in claim 9, wherein the write data transmitted to the data-in transfer storage and corresponding command data transmitted to the command transfer storage are processed when transmitted during different clock signals.

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (original) A multi-port memory controller as recited in claim 8, wherein the command transfer storage further receives a priority value indicating a priority level of the command data.

15. (original) A multi-port memory controller as recited in claim 14, wherein command data is processed based on an associated priority value.

16. (currently amended) A method for performing data transactions in a multi-port system, comprising the operations of:

receiving command data and a source id on a command channel during a first clock cycle, the source id indicating a source device that transmitted the command data;

receiving write data and a write source id at a data-in transfer storage via ~~on~~ a data-in channel during a second clock cycle, the write source id indicating a source device that transmitted the write data;

associating the command data with the write data based on the source id and the write source id; ~~and~~

transmitting both the command data and write data from the data-in transfer storage to a processing circuit for further processing during a third clock cycle when the data-in transfer storage has unused storage capacity; and

transmitting both the command data and write data via a data path that circumvents the data-in transfer storage when the data-in storage is full.

17. (original) A method as recited in claim 16, wherein the first clock cycle, second clock cycle, and third clock cycle are each separated by a plurality of clock cycles.

18. (original) A method as recited in claim 16, further comprising the operation of providing read data and a read id on a data-out channel during a fourth clock cycle, the read id indicating a source device that transmitted a read command corresponding to the read data.

19. (original) A method as recited in claim 18, further comprising the operation of associating command data with the read data based on a source id and the read id.

20. (original) A method as recited in claim 16, further comprising the operation of receiving a priority value on the command channel during the first clock cycle, wherein command data is processed based on an associated priority value.